

## **Errata: CS4353 Rev. B1 Silicon**

(Reference CS4353\_DS803A3 Data Sheet)

---

- ◆ If the VL supply is applied before the VA and VCP supplies, a DC offset will occur on the analog outputs. The offset level is bimodal: either approximately 0.7 V below the VL supply or approximately 50 mV. The first case can only occur if the VL supply is greater than approximately 1.2 V. Either offset level is removed when the VA and VCP supplies are applied. To prevent the offset from occurring, the VA and VCP supplies should be applied before or simultaneously with the VL supply.

---

### **Contacting Cirrus Logic Support**

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find the one nearest you, go to <http://www.cirrus.com>